CLAIMS

What is claimed is:

1. An automatic scan test enable signal assertion system comprising:

a scan test enable trigger sensing component adapted to provide an assertion or deassertion notification when logical values of a trigger signal captured during multiple stages provide an indication to begin a scan test enable signal assertion or deassertion; and

a staging component coupled to said scan test enable trigger sensing component, said staging component adapted to advance said logical values of said trigger signal through a plurality of stages in accordance with a progression signal and issue an asserted or deasserted scan test enable signal based upon said assertion or deassertion notification from said scan test enable trigger sensing component.

2. The automatic scan test enable signal assertion system of Claim 1 in which said trigger signal is a PCI reset signal and said stage progression signal is a PCI clock signal.

3. The automatic scan test enable signal assertion system of Claim 1 in which said trigger signal and said stage progression signal are controlled by a tester during testing operations.

4. The automatic scan test enable assertion system of Claim 1 in which said staging component further comprises:

a first stage scan enabling component coupled to said scan test enable trigger sensing component, said first stage scan enabling component adapted to track logical values of the trigger signal during a first stage;

a second stage scan enabling component coupled to said scan test enable trigger sensing component, said second stage scan enabling component adapted to track logical values of the trigger signal during a second stage;

a third stage scan enabling component coupled to said scan test enable trigger sensing component, said third stage scan enabling component adapted to maintain an active scan enable signal status until an stage progression signal permits a contrary indication to be received by said third stage scan enabling component.

5. The automatic scan test enable signal assertion system of Claim 4 in which said

progression signal is a PCI clock signal and said third stage scan enabling component delays asserting or deasserting said scan test enable signal until there is a low to high transition in said PCI clock signal permitting a change in the scan test enable signal status.

6. The automatic scan test enable signal assertion system of Claim 4 in which said scan test enable trigger sensing component includes a NAND Boolean logic component.

7. The automatic scan test enable signal assertion system of Claim 4 in which said scan test enable trigger sensing component issues a notification to said third stage scan enabling component to assert a scan test enable signal if the inverse logical value forwarded from said first stage scan enabling component and the logical value from second stage scan enabling component are logical one values.

8. The automatic scan test enable signal assertion system of Claim 4 in which said scan test enable trigger sensing component issues a notification to said third stage scan enabling component to deassert a scan test enable signal if the inverse logical value forwarded from said first stage scan enabling component or the logical value from second stage scan enabling component are not logical one values.

9. The automatic scan test enable signal assertion system of Claim 4 in which said trigger signal is set to a high logical value at a low to high transition of said stage progression signal and said trigger signal is set to a low logical value at two consecutive high to lows transitions is said stage progression.

10. The automatic scan test enable signal assertion system of Claim 4 further comprising a network interface card.

11. An automatic scan test enable signal activation system comprising:

a scan test enable signal assertion system adapted to automatically assert or deassert the scan test enable signal in response to transitions in a trigger signal and stage progression signal;

a mutliplexer (MUX) coupled to said automatic scan test enable signal assertion system, said multiplexer is adapted to facilitate transmission of signals depending upon the assertion of a scan test enable signal;

a functional component coupled to said multiplexer, said functional component is adapted to perform normal operations of an ASIC or printed circuit board;

an input port coupled to said functional component, said input port is adapted to function as input connections that communicate signals to said ASIC or said printed circuit board;

a NAND gate coupled to said input port, said NAND gate is adapted to capture information from said input port; and

a test data output port coupled to said multiplexer, said test data output port adapted to communicate test data off of said ASIC or said printed circuit board.

12. The automatic scan test enable signal activation system of Claim 11 further comprising a plurality of NAND gates coupled together to form a NAND tree scan test chain.

13. The automatic scan test enable signal activation system of Claim 11 in which said NAND tree scan chain is adapted to test inputs of an ASIC or printed circuit for open circuits and short circuits by capturing information from said inputs when said inputs are set to a logical low value and then one by one serially toggles them high and low.

14. The automatic scan test enable signal activation system of Claim 11 in which said multiplexer facilitates transmission of test data information via said test data output port when a scan test enable signal is asserted by said scan test enable signal assertion system.

15 An automatic scan test enable signal assertion method comprising the steps of:

a) transitioning logical values of a trigger signal;

b) asserting a scan test enable signal based upon logical values in said trigger signal;

c) suspending transitions in an stage progression signal;

d) deasserting said scan test enable signal if a transition occurs in said stage progression signal; and

e) utilizing a normal functional pin to communicate said trigger signal and said stage progression signal.

16 The automatic scan test enable signal assertion method of Claim 15 further comprising the step of waiting for indications from a stage progression signal before processing information in a following stage.

17 The automatic scan test enable signal assertion method of Claim 15 further comprising the step of transmitting a logical value of said trigger signal through stages determined by said stage progression signal.

18 The automatic scan test enable signal assertion method of Claim 17 in which said scan test enable signal is asserted based upon a logical value of said trigger signal in a first stage and a logical value of said trigger signal in a second stage.

19 The automatic scan test enable signal assertion method of Claim 17 in which said scan test enable signal is asserted if said trigger signal is at logical 1 value during a first stage and the trigger signal is at a logical 0 value during a second stage and third stage.

20 The automatic scan test enable signal assertion method of Claim 15 in which said trigger signal is a reset signal and said stage progression signal is a clock signal.

21 The automatic scan test enable signal assertion method of Claim 15 further comprising the steps of:

capturing logical values of said trigger signal in a first stage and a second stage;

initiating a said scan test enable indication signal based upon said captured logical values; and

forwarding a scan test enable signal in response to a stage progression signal.